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Art Unit: 2631

02106-URLX

AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A circuit for generating aligned clock and data signals, comprising:
a clock input;
a clock multiplication circuit for receiving an external clock signal from said clock input and generating a multiplied clock signal;
a first circuit path receiving ~~[[an]]~~ said external clock signal and said multiplied clock signal from said clock input, and generating an aligned clock signal; and
a second circuit path receiving said multiplied clock signal and generating an aligned data signal;
wherein said first and second circuit paths comprise identical circuit components, and said aligned clock signal generated by said first circuit path serves as a clock signal for said aligned data signal generated by said second circuit path.
2. (Currently Amended) The circuit as claimed in claim 1, wherein said first and second circuit paths each ~~comprises~~ comprise a D flip-flop for receiving said multiplied clock signal and an output buffer for buffering said aligned clock signal and said aligned data signal respectively.
3. (Cancelled).
4. (Currently Amended) The circuit as claimed in claim ~~[[3]]~~ 1, wherein said clock multiplication circuit comprises a clock multiplier and an inverter.
5. (Currently Amended) A circuit for generating aligned clock and data signals,

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comprising:

a clock input;

an inverter receiving an external clock signal from said clock input and generating an inverted clock signal;

a clock derivation circuit receiving said external clock signal and generating a derived clock signal and an inverted derived clock signal;

a first circuit path receiving said inverted clock signal ~~from said inverter and said inverted derived clock signal~~, and generating an aligned clock signal; and

a second circuit path receiving said derived clock signal and generating an aligned data signal;

wherein said first and second circuit paths comprise identical circuit components, and said aligned clock signal generated by said first circuit path serves as a clock signal for said aligned data signal generated by said second circuit path.

6. (Currently Amended) The circuit as claimed in claim 5, wherein said first and second circuit paths each comprise comprises a D flip-flop for receiving said inverted derived clock signal and said derived clock signal respectively and an output buffer for buffering said aligned clock signal and said aligned data signal respectively.

7. (Currently Amended) The circuit as claimed in claim 6, said clock derivation circuit further comprising a clock multiplier receiving said external clock signal and sending a multiplied clock signal as said derived clock signal to said D flip-flop in said second circuit path, and an inverter receiving said multiplied clock signal and sending an inverted multiplied clock signal as said inverted derived clock signal to said D flip-flop

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in said first circuit path.

8. (Currently Amended) A circuit for generating aligned clock and data signals, comprising:

a clock input;

an inverter receiving an external clock signal from said clock input and generating an inverted clock signal;

a clock derivation circuit receiving said external clock signal and generating a derived clock signal and an inverted derived clock signal;

a first circuit path receiving said inverted clock signal ~~from said inverter and said inverted derived clock signal~~, and generating an aligned clock signal;

a second circuit path receiving said inverted derived clock signal and generating an aligned data strobe signal;

a third circuit path receiving said derived clock signal and generating an aligned first data signal; and

a fourth circuit path receiving said derived clock signal and generating an aligned second data signal;

wherein said first, second, third and fourth circuit paths comprise identical circuit components, said aligned clock signal serves as a clock signal for said aligned first data signal and said aligned second data signal, and said aligned data strobe signal serves as a data strobe signal for said aligned first data signal and said aligned second data signal.

9. (Currently Amended) The circuit as claimed in claim 8, wherein said first, second, third

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and fourth circuit paths each ~~comprises~~ comprise a D flip-flop for receiving said inverted derived clock signal or said derived clock signal and an output buffer for buffering said aligned clock signal, said aligned data strobe signal, said aligned first data signal and said aligned second data signal respectively.

10. (Currently Amended) The circuit as claimed in claim 9, said clock derivation circuit further comprising a clock multiplication circuit receiving said external clock signal, sending a multiplied clock signal as said derived clock signal to said D flip-flops in said third and fourth circuit paths, and sending an inverted multiplied clock signal as said inverted derived clock signal to said D flip-flops in said first and second circuit paths.
11. (Original) The circuit as claimed in claim 10, said clock multiplication circuit comprising a clock multiplier receiving said external clock signal and sending a multiplied clock signal to said D flip-flops in said third and fourth circuit paths, an inverter receiving said multiplied clock signal and sending an inverted multiplied clock signal to said D flip-flop in said first circuit path, and an inverter receiving said multiplied clock signal and sending an inverted multiplied clock signal to said D flip-flop in said second circuit path.